A Novel Hybrid PWM Method for DC-Link Voltage Balancing in a Three Level Neutral Point Clamped Inverter

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***Abstract*— A 3-Level Neutral Point Clamped inverter plays an imperative role in high power applications with medium voltage level. However, it possess a drawback of neutral point potential variation in the converters. This paper presents an algorithm to balance the DC-link voltage in a three level neutral point clamped inverter using a hybrid PWM technique. The advantage of both carrier based PWM and Space vector approaches are combined to get the desired voltage level without compromising on the quality of voltage being supplied by the inverter. A comparative analysis of the inverter performance with and without the proposed balancing scheme is provided. In addition, total harmonic distortion of current (%THD) and the DC-link voltage balancing capabilities are also compared. It is proven that by using this scheme the harmonic distortion is well below the permissible level, thereby reducing the losses on the drive system. Simulation studies are carried using MATLAB/Simulink on a 5HP induction motor and dc-link capacitor ratings of 100 µF each.**

Keywords— Carrier based pulse width modulation (CB-PWM) DC-link capacitor, motor drives, neutral point clamped inverter (NPC), space vector pulse width modulation (SVPWM)

I. INTRODUCTION

The development in the field of power electronics has revolutionized the deployment of converters for various motor drive systems. A three level neutral point clamped inverter is used in high-voltage and high-power applications with exceptional drive system efficiency even under wide range of machine speed [1], [2].

However, a three level inverter hold a severe problem of neutral point potential variation (NPP) [3]. This may be caused due to the variation in load unbalancing, non-uniform distribution of charges in the capacitor, transients in steady state or inaccuracy in switching instants of the devices. There are many schemes developed to overcome the voltage imbalances [5]-[10].

One of the techniques used is the carrier-based PWM practice where a common mode voltage V_0 is applied to the reference phase voltages in order to balance the DC-link voltages. The DC offset voltage has to be chosen carefully as an improper value can cause the entire system to become unstable [5]. This scheme is implemented using two separate carriers which are in phase which adds to the computation complexity. However instead of using two carrier signals a single carrier signal can be used which is a modified control strategy [6].

The proposed scheme focusses on a Hybrid PWM technique which ensures the advantage of both carrier-based PWM and Space vector PWM. The pulses to the switching devices are generated using a carrier based PWM and the PWM. The advantages of H-PWM scheme is that it reduces the computational time to generate the duty cycle and avoids the use of controllers which are conventionally used for the voltage balancing.

II. PROPOSED SYSTEM

A. Block Diagram Description

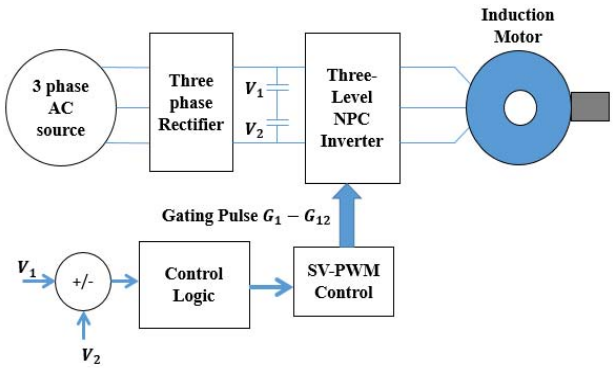

Fig. 1. Block diagram of proposed scheme.

Fig.1. shows the block diagram of the proposed system. A three phase rectifier is fed from a three phase AC source. The DC-link capacitors are V_1 and V_2 whose voltage has to be balanced. The voltage is supplied to the neutral point clamped inverter in such a way that there is an equal voltage sharing from the DC-bus. However due to the unbalanced load current, there

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is always a capacitor imbalance. This leads to the unequal voltage sharing causing a deviation in the voltage drawn by the upper and the lower DC bus. The impact of such an occurrence is crucial on the drive part as well as on the control part. There is an increased voltage stress on the switching devices, increased harmonic content in the inverter output voltage and current and torque ripple in the motor.

The three level NPC inverter drives the induction motor. The gating signals to the switches are provided by the SV-PWM technique. Until the gating pulses are provided to the switching device, the voltage balancing is not considered. Once pulses are given, the focus is on balancing the neutral point potential. This is done by the redundant voltage vector. The difference of the voltages V_1 and V_2 are evaluated, based on which the control logic is triggered.

The control logic implements the redundant vector identification block. Depending on the two capacitor voltages, the availability of redundant voltage vector is identified. If there is so, the switching states are correspondingly replaced by its positive or negative redundant states.

A reviewed gate is generated to provide the updated duty to the inverter to reduce the voltage imbalance in DC-link capacitors.

B. Space Vector Pulse Width Modulation (SV-PWM)

A three level NPC inverter is shown in Fig.2. Space vector modulation for a three level NPC inverter is shown in Fig.3. The inverter has 4 switches in each leg [4]. Each leg depicts a phase. Connected to the midpoint of the DC-link capacitor are connected 2 diodes in each leg. Hence, there exists 27 switching combinations, on which 24 are called active vectors and 3 are zero or null vectors. The former are so called since theses vectors are responsible for the power flow from source to load whereas latter are the ones which has no power flow.

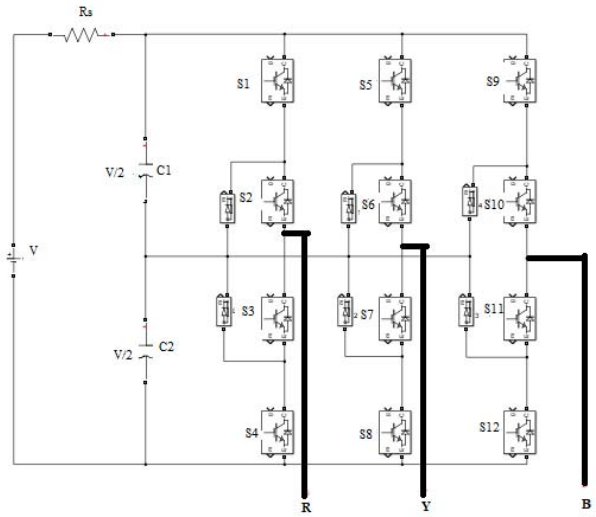

Fig. 2. Three level neutral point clamped inverter.

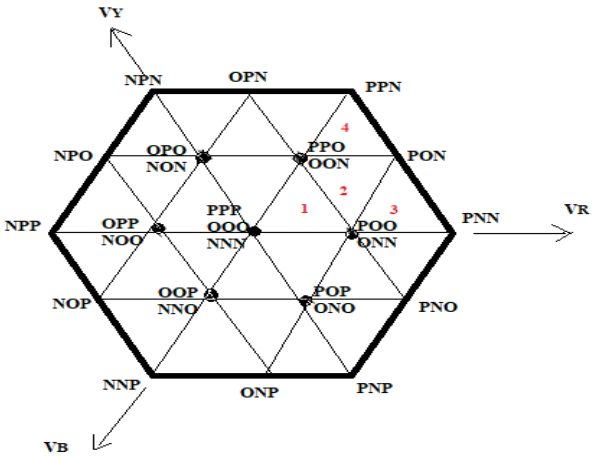

Fig. 3. Space Vector representation for a three level NPC inverter.

Table I shows the switching states and their respective pole voltages. Table II shows the various switching combinations and the voltage levels associated with it.

TABLE I
SWITCHING STATES

Switching states	S_1	S_2	S_3	S_4	Pole Voltage
P	ON	ON	OFF	OFF	+V/2
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-V/2

TABLE II
DIFFERENT SWITCHING COMBINATIONS [4]

Switching vector combination	Voltage level
PPP,NNN,OOO	0 (Null)
PPPO,OON,POO,ONN,POP,ONO,OOP,NNO,OPP, NOO,OPO,NON	V/3 (Small)
PON,OPN,NPO,NOP,ONP,PNO	V/$\sqrt{3}$ (Medium)
PNN,PPN,NPN,NPP,NNP,PNP	2V/$\sqrt{3}$ (Large)

The small and the medium voltage level vector is the reason for voltage imbalance in the DC-link as there is a neutral point connection associated with it.

The reference voltage in a 3-level inverter is produced similar

to that of a 2-level inverter. The voltage vector is generated using a combination of adjacent switching states in a particular sub-sector. For E.g. consider Fig.4.

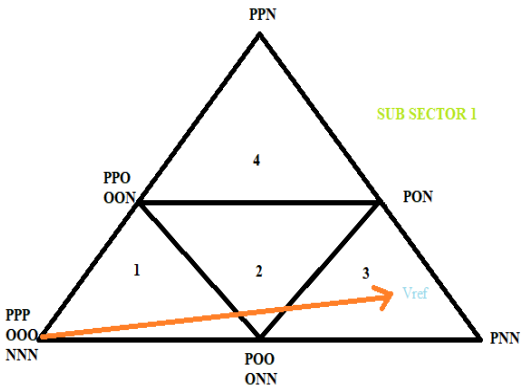

Fig. 4. Switching states in sub-sector 3.

To generate the reference voltage vector V_{ref} in sub-sector 3, the adjacent lying voltage vectors are switched; POO/ONN (V_1), PNN (V_3) and PON (V_2).

$$V_{ref}.T_s = T_1.V_1 + T_2.V_2 + T_3.V_3 \quad (1)$$

where $T_s = T_1 + T_2 + T_3$

C. Hybrid-PWM Technique

In the proposed control scheme, the advantage of both Space vector and CB-PWM technique is established and the performance is relatively superior to the conventional SV-PWM.

Table III provides the Hybrid-PWM DC-link balancing strategy. The redundant vectors identification is based on Table III. When V_1 is greater than V_2, then the positive voltage vector is switched and when V_2 is greater than V_1, then the negative voltage vector is triggered. Likewise the balancing of DC-link capacitors can be established by switching between the positive or negative voltage vectors. The positive rail is related to the upper capacitor and negative rail is related to the lower capacitor.

III. SIMULATION TEST RESULTS

Simulation studies were carried out in MATLAB/Simulink in an induction motor with motor rating of 5HP, 460V, 1750RPM, 50Hz.The DC-link voltage was kept at 600 V with capacitor ratings of 100µF each. A high switching frequency of 10 KHz was established. The modulation index was maintained at 0.8.Table IV shows the motor parameters used for simulation.

TABLE III
HYBRID -PWM DC-LINK VOLTAGE BALANCING SCHEME [1]

Redundant State	Balancing Ability	Switching State
POO	V1>V2	POO
	V2>V1	ONN
ONN	V1>V2	POO
	V2>V1	ONN
PPO	V1>V2	PPO
	V2>V1	OON
OON	V1>V2	PPO
	V2>V1	OON
OPO	V1>V2	OPO
	V2>V1	NON
NON	V1>V2	OPO
	V2>V1	NON
OPP	V1>V2	OPP
	V2>V1	NOO
NOO	V1>V2	OPP
	V2>V1	NOO
OOP	V1>V2	OOP
	V2>V1	NNO
NNO	V1>V2	OOP
	V2>V1	NNO
POP	V1>V2	POP
	V2>V1	ONO
ONO	V1>V2	POP
	V2>V1	ONO
PON,OPN,NPO, NOP,PNO,ONP	V1>V2	PON,OPN,NPO, NOP,ONP,PNO
	V2>V1	
PNN,PPN,NPN, NPP,NNP,PNP	V1>V2	PNN,PPN,NPN, NPP,NNP,PNP
	V2>V1	

TABLE IV
MOTOR PARAMETERS

IM rating, Line Voltage	5 HP,460 V
Stator Resistance (R_s) and Stator Inductance (L_{ls})	1.115Ω, 0.005974H
Mutual Inductance (L_m)	0.2037H
Inertia(J)	0.02kg.m^2
Pole pairs (P)	2
Rated Speed (N)	1750

Fig.5. shows the simulation of the proposed scheme. The SVPWM block feeds the pulse required by the twelve switches in the inverter

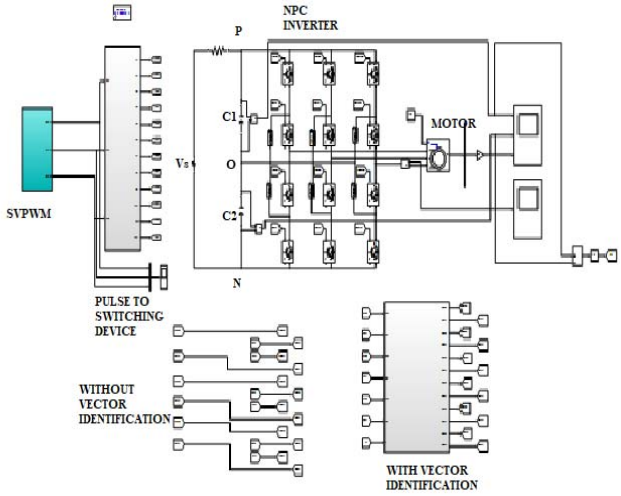

Fig. 5. Simulation of the proposed scheme.

In order to compare the performance of the motor, blocks entitled “with vector identification” and “without vector identification” is provided.

The simulation for pulse generation through SVPWM shown in Fig.6.

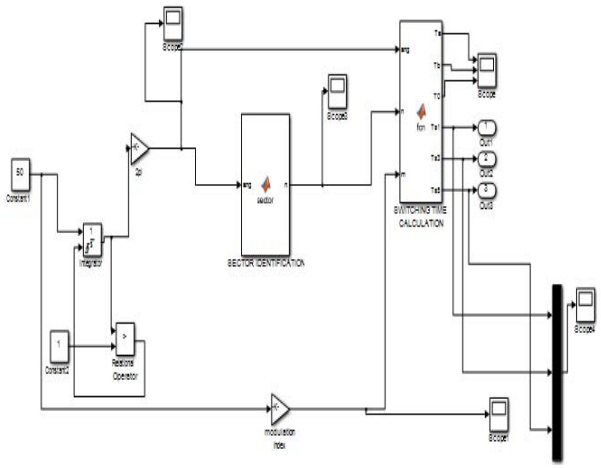

Fig. 6. Simulation of SVPWM.

Fig.7. shows the simulation result of the pulses to one of the inverter legs (R-phase).Fig.8. shows the capacitor imbalance .It can be observed that while the voltage across the upper (positive) DC capacitor is diminishing to zero the lower (negative) bus attains the full supply voltage of 600V.Fig.9.shows the corresponding impact on the speed, torque and stator current of the induction motor.

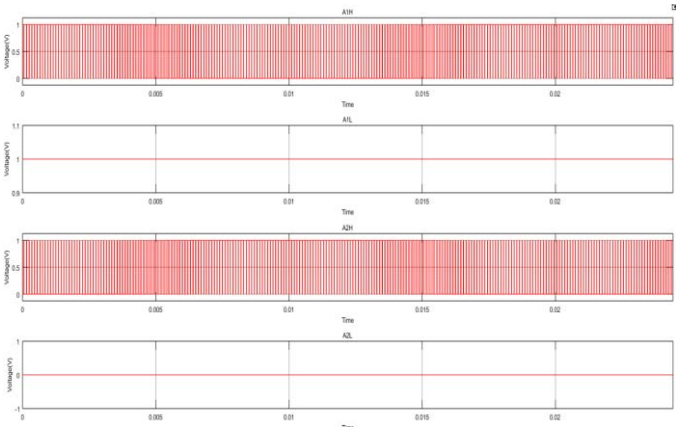

Fig.7. Gate pulse to R-phase.

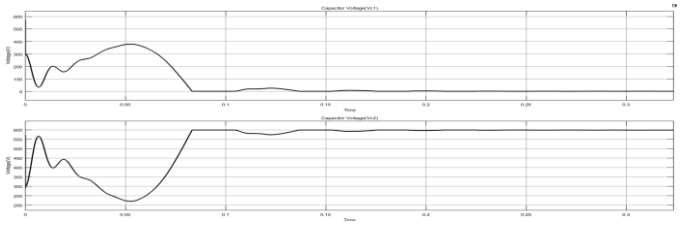

Fig.8. DC-link Capacitor imbalance before redundant vector identification.

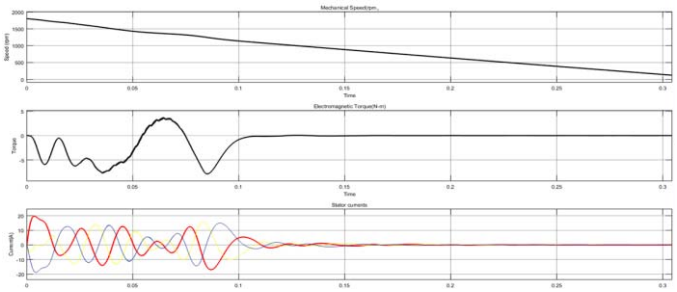

Fig.9.Torque, speed and stator current of the motor

Once the vector identification is performed, there is a significant change in the motor performance and the balancing capability of the capacitor also improves largely.

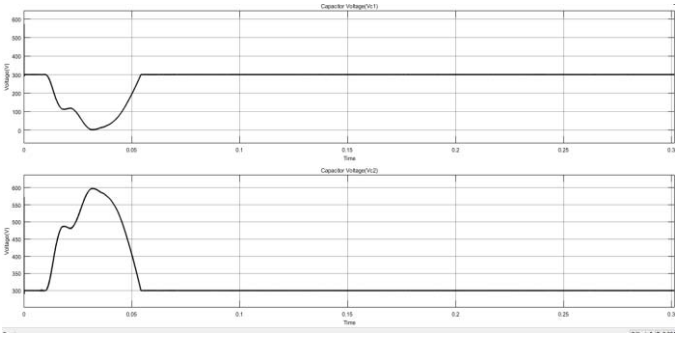

Fig.10.DC-link capacitor balancing after vector identification.

Fig.10. shows the capacitor balancing capability after vector identification. It is clear that both the capacitor shares an equal voltage of 300V after the balancing scheme is implemented.

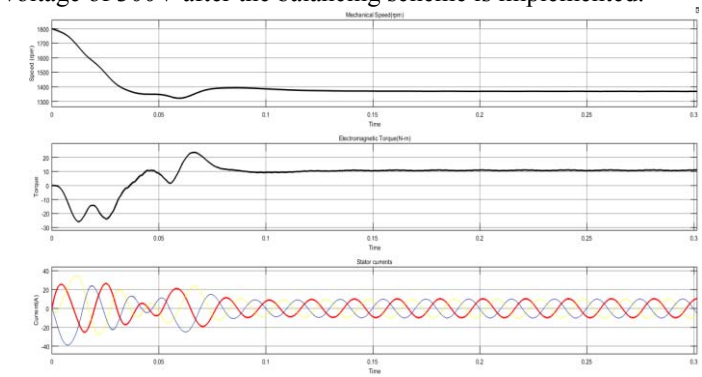

Fig.11.Torque, speed and stator current of the motor after capacitor balancing.

Fig.11. shows the improved torque and speed characteristics of the induction motor with a sinusoidal three phase stator current of the motor.

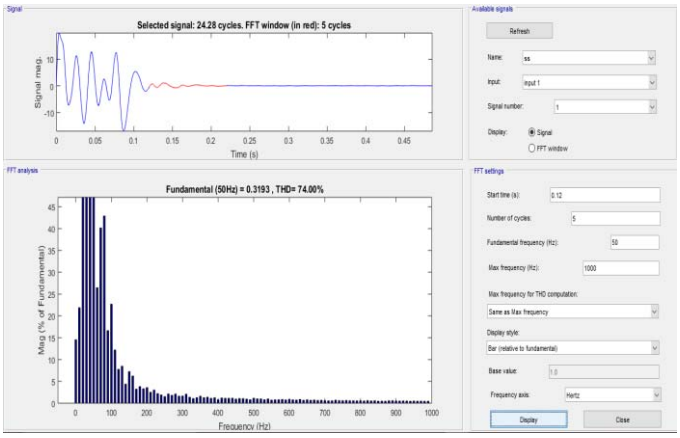

Fig.12.Simulated stator phase current and its frequency spectrum with capacitor unbalancing.

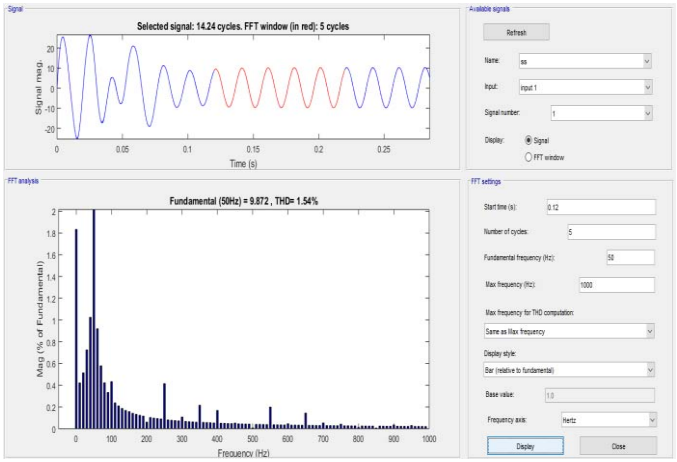

Fig.13.Simulated stator phase current and its frequency spectrum with capacitor balancing.

Fig.12. and Fig.13. shows a comparison of the frequency spectrum of the stator phase current with capacitor unbalancing and capacitor balancing respectively. The THD content in unbalanced condition is 74% which is very large whereas under balanced condition the %THD is 1.54 which is well below the permissible value of 5%.

IV. CONCLUSION

The concept of redundant vector identification used in Hybrid-PWM makes the scheme simpler compared to the computational complexity otherwise seen in conventional SV-PWM. Voltage balancing of the DC-link can be achieved without using any complex circuits or controllers, which further reduces the cost of the system. Detailed simulation compares the motor performance and stator phase currents. The balancing capabilities using the Hybrid PWM is also studied. The scheme reduces the distortion in voltage, current and improves the speed torque characteristics of the motor.

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