Course Code	Course Name	L-T-P- C	Year of Introduction
06EC6025	<b>Analog Integrated Circuit Design -1</b>	4-0-0-4	2015

## **Course Objectives**

To give the Student an idea about:-

- 1. The operation of the MOS transistor
- 2. Understand the behaviour of the MOS transistor in circuits
- 3. Understand how MOS transistors are modelled for CAD tools
- 4. The analysis of the Single stage amplifiers

## **Syllabus**

Operation and modeling of MOS transistor; Short channel effects and modelling of MOS devices; Noise and frequency response analysis of single stage amplifiers.

## **Course Outcome**

Students who successfully complete this course will be able to analyze quantitatively the behaviour of MOS transistor in various regions of operation; use the time domain and frequency domain concepts in analysing the circuits; to design a CMOS based system, component, or process within realistic constraints.

## **Text Books**

- 1. YannisTsividis and Colin McAndrew, "Operation and Modeling of the MOS Transistor", 3/e, 2010, OUP.
- 2. R. Jacob Baker, Harry W Li, David E Boyce, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, 1998.
- 3. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill 2008.
- 4. Philip E Allen, Douglas R Holberg, "CMOS Analog Circuit Design" International Student(Second) Edition, First Indian Edition 2010.

Course Plan				
Module	Content	Hours	Sem. Exam	

2-Terminal MOS Structure - F  Balance and Charge, Effect of Ga  Condition General Analysis.  approximation, Strong and Weal  Capacitance.  3-Terminal MOS Structure - General Analysis, Body-effect, Pin Regions of Operation.	Inversion: charge sheet k Inversion, Small Signal Contacting Inversion Layer,	14	25
Condition General Analysis.  approximation, Strong and Weal Capacitance.  3-Terminal MOS Structure - General Analysis, Body-effect, Pin	Inversion: charge sheet k Inversion, Small Signal  Contacting Inversion Layer,	14	25
approximation, Strong and Weal Capacitance.  3-Terminal MOS Structure - General Analysis, Body-effect, Pin	k Inversion, Small Signal  Contacting Inversion Layer,	14	25
Capacitance.  3-Terminal MOS Structure - General Analysis, Body-effect, Pin	Contacting Inversion Layer,	14	25
General Analysis, Body-effect, Pin	•		
General Analysis, Body-effect, Pin	•		
	nch-off voltage. Introduction,		
4-Terminal MOS Structure –			
Introduction, Complete All-Region	Model - Current Equations,		
Simplified All-Region Models: Li	0 1		
Charge, Source-Referenced Simplifie	ed All- Region Models.	14	25
INTERNAL T	TEST 1		
Strong Inversion: Complete	Strong Inversion Model-		
NonSaturation, Source-Referenced Models	Simplified Strong Inversion		
Short Channel Effects: Scaling	Theory, Threshold Voltage		
Variation, Mobility Degradation w	vith Vertical Field, Velocity		
Saturation, Hot Carrier Effects.			
MOS Device Models: Level 1 Mo	odel, Level 2 Model, Level 3		
Model , BSIM Series, Other Mo	odels, Charge and Capacitor		
III Modeling, Temperature Dependence.		12	25
Noise: Statistical Characteristics	of Noise, Noise Spectrum,		
Amplitude Distribution, Correlated			
Types of Noise: Thermal, Flicker, S Noise in Circuits.	Shot Noise Representation of		
INTERNAL	TEST 2		
Single-Stage Amplifiers - Intro- Configurations - Resistive Load	duction to basic amplifier		
IV Active Loads: Gate-Drain Connect Frquency Response, Noise Analysis, and CG, Frequency Response, Noise	Current-Source Load: CS, CD	12	25

	Cascode, Folded Cascode, Push-pull amplifier- Noise Analysis			
END SEMESTER EXAM				